

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

REMARKS

Claims 1 – 17 are pending.

Claims 7 - 14 have been amended and claims 15-17 are added as new claims in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The Applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **April 23, 2003**.

Claim Rejection - 35 USC §112

Claims 7-14 are rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Taking the Examiner's comments into consideration claims 7 and 14 have been amended. Therefore, withdrawal of the rejection of Claims 7-14 under 35 USC §112, first paragraph, is respectfully requested.

Claim Rejection - 35 USC §103

Claims 7-14 are rejected under 35 USC §103(a) as being unpatentable over Harada et al. (U.S. Patent No. 6,417,575 B2) in view of Yamaha (U.S. Patent No. 6,297,563 B1).

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer

insulating film (7) a first intra-layer insulating film (11). Please note that the pad portion of this device is wider than the wiring portion.

Yamaha describes a semiconductor device having a second-level interlayer insulating film (22) provided to prevent peel-off and cracks from forming

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to $2 \times W2 + n \times W3$ as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3 corresponds to the distance P2. Please note that the variable n is not defined in the specification. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio L1/W1 is 30 percent or higher.

The Examiner asserts that Yamaha shows a plurality of insulating regions (portions of insulating layer 22 between plugs 22b). This assertion is respectfully traversed.

In the present invention, a recess and a plurality of insulating regions are formed. For example, as shown in Fig.2A, a plurality of insulating regions 21a are disposed, and the pad 27 filled in the recess is a clump of conductive material.

The pad 27 is not divided into some pieces. In contrast, as shown in Yamaha's

Fig.2, a plurality of plugs 22B (recess) shown in Fig.1 are disposed. In Yamaha's Fig.1, it appears that there are a plurality of insulating regions. However, in Fig.2, the insulating regions are connected with each other. Namely, Yamaha does not disclose *a* recess and a *plurality* of insulating regions, but discloses *a plurality of* recesses and *an* insulating region.

Furthermore, as shown in Yamaha's Fig.2, the plugs 22B are not arranged in an area adjacent to the edge of the pad. The area adjacent to the edge of the pad is an insulating region. Furthermore, the plugs 22B are arranged uniformly. In contrast, in claim 14, an area ratio of the recess in the first frame area is larger than that in the second frame area. Yamaha does not disclose such structure.

Therefore, claims 7, 9 and 14 patentably distinguish over the prior art relied upon, by recting, as exemplified by claim 7,

"A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions being protruded from the bottom of the pad part, and the recess being formed so that the insulating regions are disposed in such a manner that an area ratio of the recess in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than an area ratio of the recess in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess.

Therefore, withdrawal of the rejection of Claims 7-14 under 35 USC §103(a) as being unpatentable over Harada et al. (U.S. Patent No. 6,417,575 B2) in view of Yamaha (U.S. Patent No. 6,297,563 B1) is respectfully requested.

Application No. 10/050,171
Atty. Docket No. 020029

New Claims

New claims 15-17 are added to the application. New claims 15-17 find support in the specification. Claims 15-17 patentably distinguish over the prior art relied upon by reciting, as exemplified by claim 16,

“A semiconductor device comprising: a semiconductor substrate; a first interlayer insulating film made of insulating material and formed on the semiconductor substrate; a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of insulating regions being protruded from the bottom of the pad part, and the recess being formed so that the insulating regions are disposed in such a manner that a square measurement of the recess in the near wiring area divided by a total square measurement of the recess in the second frame area divided by a total square measurement of the second frame area in a near wiring area superposed upon an extended area of the wiring part into the pad part, within the first frame area having as an outer periphery and outer periphery of the pad part and having a first width, becomes larger than a square measurement of the recess in the near wiring area divided by a total square measurement of the recess in the second frame area divided by a total square measurement of the second frame area in a second frame area having as an outer periphery and inner periphery of the first frame are and having a second width; a first pad filled in the pad part of the recess; and a wiring filled in the wiring part of the recess.”
(Emphasis Added)

Therefore, allowance of new claims 15-17 is respectfully requested.

Application No. 10/050,171
Atty. Docket No. 020029

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/anp

Atty. Docket No. 020029
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



23850

PATENT TRADEMARK OFFICE

Q:\HOME\GSTEVENS\02\020029\amendment July 2003.rtf